CLAIMS

What is claimed is:

1. An integrated circuit fabricated on a chip, comprising:

at least one source device in the integrated circuit generating internal state data at a first frequency;

an output port that drives data to external logic at a second frequency that is lower than said first frequency; and

wherein said output port includes a bandwidth manager that selects internal state data that is most important to drive to said external logic during periods when said output port becomes saturated, and which selects all internal state data to drive to said external logic during periods when said output port is not saturated .

2. The system of claim 1, wherein the integrated circuit comprises a processor, and multiple internal data sources generate internal state data.

3. The system of claim 2, wherein the internal state data sources are organized by regions within the processor, and internal state data from one or more of the regions are selected by a user programmable enable signal.

4. The system of claim 3, further comprising a data source multiplexer that selects said one or more regions based on said user programmable enable signal.

5. The system of claim 2, wherein multiple output ports are provided in said processor, at least one of which includes a bandwidth manager.

6. The system of claim 2, wherein output port includes an output driver that drives internal state data selected by the bandwidth manager to said external logic.

7. The system of claim 6, wherein the bandwidth manager includes selection logic that selects data from one or more sources to pass to said output driver.

8. The system of claim 7, wherein the selection logic comprises a multiplexer.

9. The system of claim 7, wherein the selection logic assigns an importance level to each tick of said internal state data, which is used by said bandwidth manager to determine whether the tick should be selected for transmission to external logic when the output port is saturated.

10. The system of claim 9, wherein the selection logic adds at least one control bit to each tick indicating the importance level of that tick.

11. The system of claim 9, wherein the selection logic also adds a control bit to each tick indicating if the tick represents valid data.

12. The system of claim 11, wherein the bandwidth manager further includes a smart buffer coupled to said selection logic, and wherein said selection logic presents a tick to said smart buffer at said first frequency.

13. The system of claim 12, wherein the smart buffer has a plurality of slots for storing ticks, and wherein said smart buffer periodically unloads a tick at the second clock frequency to pass to said output driver.

14. The system of claim 13, wherein the smart buffer is configured as a first-in, first-out memory buffer, and wherein said smart buffer accepts the tick presented by said selection logic if a first slot in said smart buffer is empty.

15. The system of claim 14, wherein the smart buffer accepts the tick presented by said selection logic if the smart buffer is concurrently unloading a tick to pass to said output driver.

16. The system of claim 14, wherein the smart buffer accepts the tick presented by said selection logic if the importance level of the presented tick is greater than the importance level of the tick stored in the first slot of said memory buffer, and wherein said smart buffer overwrites the value of the presented tick in said first slot.

17. The system of claim 14, wherein the smart buffer determines if any slots are empty, and if so, advances ticks stored in full slots to fill the empty slots.

18. The system of claim 17, wherein the full ticks are advanced on at a rate equal to said first frequency.

19. The system of claim 14, wherein a plurality of smart buffers are included in said bandwidth manager which are connected in parallel to process data concurrently.

20. The system of claim 19, wherein the selection logic is capable of presenting a tick to each of said plurality of said smart buffers at a rate equal to said first frequency.

21. The system of claim 20, wherein the bandwidth manager further includes arbitration logic coupled to a last slot of each of said plurality of smart buffers, and wherein said arbitration logic selects the tick stored in the last slot of one of said smart buffers to unload at said second clock frequency.

22. The system of claim 20, wherein the arbitration logic receives a signal indicating the importance of the tick in the last slot of each smart buffer, whether the last slot of each smart buffer is full, and whether each smart buffer is under pressure.

23. The system of claim 22, wherein the arbitration logic selects the last tick from a smart buffer if it is under pressure and the other smart buffer(s) is not.

24. The system of claim 22, wherein the arbitration logic selects the last tick which has the highest importance level.

25. The system of claim 21, wherein the arbitration logic selects the last tick from said plurality of said smart buffers on a round-robin basis.

26. The system of claim 1, wherein the first frequency is the frequency of the selected source.

27. The system of claim 26, further comprising a clock circuit that automatically determines the second frequency based on the ratio of the first frequency to an internal system clock.

28. The system of claim 27, wherein the clock circuit rounds up the ratio to an integer value to reduce the second frequency.

29. The system of claim 1, wherein the bandwidth manager includes packet prediction logic which predicts the start of a packet of internal state data, and which assigns an importance value to each tick of said packet based on the location of the tick in the packet.

30. The system of claim 29, wherein the packet prediction logic includes a decoder that decodes opcodes in a first tick of a packet to identify the length of each packet.

31. The system of claim 29, wherein the packet prediction logic synchronizes when a packet pattern is detected from said source device.

32. A processor, comprising:

a plurality of internal source devices generating internal state data at a first frequency;

an output driver that drives data to external logic at a second frequency; and

a bandwidth manager that selects internal state data that is most important to drive to said external logic during periods when said output port becomes saturated, and which selects all internal state data to drive to said external logic during periods when said output driver is not saturated.

33. The processor of claim 32, wherein the internal state data sources are organized by regions within the processor, and internal state data from one or more of the regions are selected by a user programmable enable signal.

34. The processor of claim 32, wherein multiple sets of output drivers and bandwidth managers are provided in said processor.

35. The processor of claim 32, wherein the bandwidth manager includes selection logic that selects data from one or more sources to pass to said output driver.

36. The processor of claim 35, wherein the selection logic assigns an importance level to each tick of said internal state data, which is used by said bandwidth manager to determine whether the tick should be selected for transmission to external logic when the output driver is saturated.

37. The processor of claim 36, wherein the selection logic adds at least one control bit to each tick indicating the importance level of that tick.

38. The processor of claim 37, wherein the selection logic also adds a control bit to each tick indicating if the tick represents valid data.

39. The processor of claim 38, wherein the bandwidth manager further includes a smart buffer coupled to said selection logic, and wherein said selection logic presents a tick to said smart buffer at said first frequency.

40. The processor of claim 12, wherein the smart buffer has a plurality of slots for storing ticks, and wherein said smart buffer periodically unloads a tick at the second clock frequency to pass to said output driver.

41. The processor of claim 40, wherein the smart buffer is configured as a first-in, first-out memory buffer, and wherein said smart buffer accepts the tick presented by said selection logic if a first slot in said smart buffer is empty.

42. The processor of claim 41, wherein the smart buffer accepts the tick presented by said selection logic if the smart buffer is concurrently unloading a tick to pass to said output driver.

43. The processor of claim 41, wherein the smart buffer accepts the tick presented by said selection logic if the importance level of the presented tick is greater than the importance level of the tick stored in the first slot of said memory buffer, and wherein said smart buffer overwrites the value of the presented tick in said first slot.

44. The processor of claim 41, wherein the smart buffer determines if any slots are empty, and if so, advances ticks stored in full slots to fill the empty slots.

45. The processor of claim 44, wherein the full ticks are advanced on at a rate equal to said first frequency.

46. The processor of claim 41, wherein a plurality of smart buffers are included in said bandwidth manager which are connected in parallel to process data concurrently.

47. The processor of claim 46, wherein the selection logic is capable of presenting a tick to each of said plurality of said smart buffers at a rate equal to said first frequency.

48. The processor of claim 47, wherein the bandwidth manager further includes arbitration logic coupled to a last slot of each of said plurality of smart buffers, and wherein said arbitration

logic selects the tick stored in the last slot of one of said smart buffers to unload at said second clock frequency.

49. The processor of claim 48, wherein the arbitration logic receives a signal indicating the importance of the tick in the last slot of each smart buffer, whether the last slot of each smart buffer is full, and whether each smart buffer is under pressure.

50. The processor of claim 49, wherein the arbitration logic selects the last tick from a smart buffer if it is under pressure and the other of said plurality of smart buffers are not.

51. The processor of claim 49, wherein the arbitration logic selects the last tick which has the highest importance level.

52. The processor of claim 49, wherein the arbitration logic selects the last tick from said plurality of said smart buffers on a round-robin basis.

53. The processor of claim 32, wherein the first frequency is the frequency of the selected source.

54. The processor of claim 53, further comprising a clock circuit that automatically determines the second frequency based on the ratio of the first frequency to an internal processor clock.

55. The processor of claim 54, wherein the clock circuit rounds up the ratio to an integer value to reduce the second frequency.

56. The processor of claim 43, wherein the selection logic includes packet prediction logic which predicts the start of a packet of internal state data, and which assigns said importance value to each tick of said packet based on the location of the tick in the packet.

57. The processor of claim 56, wherein the packet prediction logic includes a decoder that decodes opcodes in a first tick of a packet to identify the length of each packet.

58. The processor of claim 57, wherein the packet prediction logic synchronizes when a packet pattern is detected from said source device.

59. An integrated circuit fabricated on a chip, comprising:

at least two source devices in the integrated circuit, each of which is capable of generating internal state data at a first frequency;

an output port that drives data to external logic at said first frequency; and

wherein said output port includes a bandwidth manager that selects internal state data that is most important to drive to said external logic during periods when said output port becomes saturated, and which selects all internal state data to drive to said external logic during periods when said output port is not saturated .

60. An integrated circuit fabricated on a chip, comprising:

at least one source device in the integrated circuit generating internal state data at a first frequency;

an output port that drives data to external logic at a second frequency; and

wherein said output port includes at least one smart buffer that examines each newly presented tick of internal state data and determines the relative importance of that tick as compared to the relative importance of the last previously stored tick.

61. The system of claim 60, wherein the smart buffer permits more important ticks to advance through the smart buffer with a tail-eating type of action in instances where the output port becomes saturated.

62. The system of claim 60, wherein the smart buffer permits all valid ticks to advance through the smart buffer in instances where the output port is not saturated.

63. The processor of claim 60, wherein the second frequency is substantially less than said first frequency.

64. The processor of claim 60, wherein the second frequency is substantially the same as the first frequency.

65. The processor of claim 32, wherein the second frequency is substantially less than said first frequency.

66. The processor of claim 32, wherein the second frequency is substantially the same as the first frequency.